What Is Claimed Is:

1.

A probe card assembly comprising a programmable controller to control the provision of

test signals to test probes of the probe card for testing components on a wafer.

2. A probe card assembly of claim 1, wherein the programmable controller comprises a

Field Programmable Gate Array (FPGA).

3. The probe card assembly of claim 1, wherein the programmable controller is connected

through an interface to a test system controller, where the test system controller provides test

signals to the interface to control testing of components on a wafer.

4. The probe card assembly of claim 3, wherein the interface comprises one or more of a

group consisting of a serial, parallel, wireless, network, RF and IR interface.

5. The probe card assembly of claim 1, further comprising a memory accessible by the

programmable controller, wherein the memory stores a test program enabling the programmable

controller to perform testing of components on the wafer.

6. The probe card assembly of claim 1, wherein the programmable controller comprises a

serial to parallel converter configured to receive the test signals, the programmable controller

configured to convert the test signals from serial to parallel and distribute the test signals in

parallel to the test probes.

Attorney Docket No.: FACT-01005US0 TAW

Express Mail No: EL 977910562 US -22taw/fact/1005/1005.001 P208-US

7. The probe card assembly of claim 1, wherein programmable controller is configured to

perform self testing of components included in the probe card assembly.

8. A probe card assembly of claim 1 further comprising:

a serial to parallel converter connected to receive signals from the programmable

controller, the serial to parallel converter being configured to convert the test signals from serial

to parallel and distribute the test signals in parallel to the test probes.

9. A probe card assembly of claim 1 further comprising:

a serial digital to analog converter connected to receive digital test signals from the

programmable controller, the digital to analog converter configured to convert and provide the

test signals to the test probes in analog form.

10. A probe card assembly of claim 1 further comprising:

a daughter card connected to a base PCB, the base PCB including the programmable

controller and connectors for connecting to a test system controller and routing lines from the

connectors to contacts providing electrical connections to the test probes for contacting DUTs on

a wafer, the daughter card supporting discrete components configured for providing additional

signals to the DUTs.

11. The probe card assembly of claim 10, wherein the discrete components comprise an

additional programmable controller.

taw/fact/1005/1005.001

-23-

P208-US

The probe card assembly of claim 10, wherein the daughter card further comprises: 12.

power supply isolation devices connected in series with multiple power supply lines that

distribute power from a single power supply line of a test system controller to multiple test

probes, each test probe configured to contact a DUT power supply input, wherein the power

supply isolation devices are configured to minimize current flow on a given one of the power

supply lines when a DUT on the given line is determined to be faulty.

13. The probe card assembly of claim 10, wherein the components on the wafer include

microprocessors, and wherein the discrete components comprise support circuits for a personal

computer motherboard.

taw/fact/1005/1005.001

A probe card assembly of claim 1 further comprising: 14.

a daughter card connected to a base PCB, the base PCB including connectors for

connecting to a test system controller and routing lines from the connectors to contacts providing

electrical connections to the test probes for contacting DUTs on a wafer, the daughter card

supporting the programmable controller.

15. A probe card assembly of claim 1 further comprising:

a space transformer supporting the test probes and having internal routing lines connected

to the test probes, wherein the space transformer supports the programmable controller.

16. A probe card assembly of claim 1 further comprising:

Express Mail No: EL 977910562 US Attorney Docket No.: FACT-01005US0 TAW -24-P208-US

resistors, each of the resistors connected in series between a single test system controller

channel and a plurality of test probes thus providing resistive isolation of the test probes.

17. A probe card assembly comprising:

isolation buffers, each of the isolation buffers connected in series between a single tester

channel and a plurality of test probes thus providing isolation of the test probes.

18. The probe card assembly of claim 2, wherein a test program loaded into the FPGA is

provided from a CAD design system used to develop the components on the wafer.

19. The probe card assembly of claim 5, wherein the test program loaded into the memory is

provided from a CAD design system used to develop the components on the wafer.

20. A probe card assembly comprising:

a daughter card connected to a base PCB, the base PCB including connectors for

connecting to a test system controller and routing lines from the connectors to contacts providing

electrical connections to test probes for contacting DUTs of a wafer, the daughter card including

discrete components configured for providing additional signals to the DUTs.

21. The probe card assembly of claim 20, wherein the daughter card is connected to the PCB

by removable connectors.

Attorney Docket No.: FACT-01005US0 TAW

Express Mail No: EL 977910562 US -25taw/fact/1005/1005.001 P208-US

22. The probe card assembly of claim 20, wherein the DUTs on the wafer include

microprocessors, and wherein the discrete components comprise support circuits for a personal

computer motherboard.

23. The probe card assembly of claim 20, wherein the discrete components comprise support

components for use in a circuit with the DUTs.

24. A probe card assembly comprising:

power supply isolation devices connected in series with multiple power supply lines that

distribute power from a single power supply line of a test system controller to multiple test

probes, each test probe configured to contact a DUT power supply input, wherein the power

supply isolation devices are configured to minimize current flow on a given one of the power

supply lines when a DUT on the given line is determined to be faulty.

25. The probe card assembly of claim 24, wherein the power supply isolation devices

comprise one or more of a group consisting of voltage regulators, switches and current limiters.

26. The probe card assembly of claim 24 comprising:

a space transformer supporting the test probes;

at least one daughter card; and

a base PCB electrically interconnected with the space transformer and the at least one

daughter card, wherein the power supply isolation devices are provided on at least one of the

space transformer, the base PCB, and the at least one daughter card.

Attorney Docket No.: FACT-01005US0 TAW taw/fact/1005/1005.001

Express Mail No: EL 977910562 US P208-US

-26-

27. A probe card assembly comprising:

a DC-DC converter connected between the single power supply line of a test system

controller, the power supply line distributing power through line branches to multiple test

probes, the DC-DC converter configured to increase current in a signal provided on the power

supply line.

28. A probe card assembly comprising a programmable controller configured to perform self

testing of components included in the probe card assembly.

29. A probe card assembly comprising a serial interface device configured to connect to a test

system controller to receive test signals for distributing to probes of the probe card assembly.

30. The probe card assembly of claim 29, further comprising:

a serial to parallel converter for converting the test signals from serial to parallel and

distributing the test signals in parallel to a plurality of test probes.

31. The probe card assembly of claim 30, wherein the serial to parallel converter comprises a

Field Programmable Gate Array (FPGA).

32. The probe card assembly of claim 31 comprising:

a space transformer supporting the test probes;

taw/fact/1005/1005.001

-27-

P208-US

at least one daughter card; and

a base PCB electrically interconnected with the space transformer and the at least one

daughter card, wherein the serial to parallel converter is provided on at least one of the space

transformer, the base PCB, and the at least one daughter card.

33. A probe card assembly comprising:

a serial digital to analog converter configured to serially receive digital test signals that

are to be distributed to test probes of the probe card in analog form, the digital to analog

converter configured to convert and provide the test signals to the test probes in analog form.

34. The probe card assembly of claim 33, further comprising:

an analog to digital converter configured to receive an analog signal from a test device

and to send a digital representation to a test system controller.

35. The probe card assembly of claim 34 comprising:

a space transformer supporting the test probes;

at least one daughter card; and

a base PCB electrically interconnected with the space transformer and the at least one

daughter card, wherein the serial digital to analog converter and the analog to digital converter

are each provided on at least one of the space transformer, the base PCB, and the at least one

daughter card.

-28-